Original Article

Low power organic field effect transistors with copper phthalocyanine as active layer

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ABSTRACT

Bottom gate, top contact Organic Field Effect Transistors (OFETs) were fabricated using copper phthalocyanine (CuPc) as an active layer. The electrical properties of OFETs fabricated with CuPc annealed at different annealing temperatures and different channel length to width (L/W) ratios were studied. The transfer characteristics of the devices appear to improve with annealing temperature of CuPc and increasing L/W ratios of the devices. Upon annealing, the field effect mobility increased from 0.03 ± 0.004 cm²/Vs to 1.3 ± 0.02 cm²/Vs. Similarly, the interface state density reduced from 5.14 ± 0.39 × 10¹¹ cm⁻²eV⁻¹ for the device fabricated using as deposited CuPc, to 2.41 ± 0.05 × 10¹¹ cm⁻²eV⁻¹ for the device with CuPc annealed at 80 °C. The on/off current ratio increased from 10² for the as-deposited device, to 10⁴ for the device with CuPc annealed at 80 °C. The dependence of the subthreshold swing on the L/W ratio was also investigated.

1. Introduction

The major challenge in the realization of low power organic field effect transistors (OFETs) is the reduction of the manufacturing cost, especially when scaling up to meet industrial demands. Low leakage current, reduction in power consumption, high mobility, light-weight and low-cost are the advantages of organic thin film transistors (OTFTs). An efficient way to reduce the overall size of the device is the use of thin inorganic dielectric and organic semiconducting layers. Even though a large spectrum of organic semiconductors has been proposed for the fabrication of OFETs, only a few can meet the requirements for electronic device applications in terms of processibility and stability in normal atmosphere. There has been a growing interest in developing new organic channel materials in order to fabricate the electronic devices. OFETs provide two principal advantages over field effect transistors (FETs) based on inorganic semiconductors. Firstly, they can be fabricated at lower temperature and lower cost.

Among various organic materials that have been extensively studied for FET applications, phthalocyanines are organic dyes that attained a lot of research interests. These materials have potential applications for various electronic components such as thin film transistors (TFTs), light emitting diodes (LEDs) etc. In this work, TFTs fabricated with a typical p-type organic semiconducting material, copper phthalocyanine (CuPc), are used as the channel material for OFET fabrication. CuPc based TFTs have shown better current saturation and high field effect mobility. Due to its good chemical stability and heat resistance, CuPc thin films can be fabricated using physical vapour deposition techniques, which is ideal from the perspective of scaling up with good uniformity for large area electronics. In addition, CuPc has good stability in ambient conditions. CuPc is a stable compound, normally found with a monoclinic crystal structure. The solubility of CuPc in common organic solvents is very less, but due to its thermal stability, uniform films can be fabricated using thermal evaporation technique, which allows industrial level scaling up. Fig. 1 shows the molecular structure of CuPc.

The dielectric material plays a crucial role in device operation since it influences the electric field, current leakage through the gate insulator and the quality of the interface between the organic semiconductor and gate dielectric. Organic dielectric materials show high leakage current with decreasing the film thickness and...
most of them do not exhibit high dielectric constant. The use of inorganic dielectrics can resolve this issue [9,10]. There are several approaches to improve the performance of OFET devices. Especially, the use of thinner high dielectric constant materials as the gate insulator is the effective way to reduce the operating voltage [11–13]. In this work, we employed a 50 nm thick silicon dioxide (SiO2) as the gate insulator, which allows us to quantify the space-charges that influence the device performance as will be discussed later in this paper. Compared to the conventional OFETs that work at large operating voltages, large threshold voltages and having low mobility [14], our devices work at much lower operating voltages with marginal threshold voltage and reasonably good carrier field effect mobility.

In this paper, we report on the fabrication of low power CuPc based OFET devices and their performance at various fabrication conditions and experimental temperatures. The electrical characteristics of the OFETs were done to estimate the device parameters such as mobility, threshold voltage, on/off current ratio, sub-threshold swing and interface trap density. The influence of the channel length – to – width ratio (L/W) and annealing temperatures on the device characteristics have been analyzed in this work.

2. Experimental

The bottom gate, top contact p-type OFETs were fabricated on a silicon wafer with CuPc as the channel layer. The bottom gate structures are usually used in OFETs because organic semiconductors are more prone to damage during conventional manufacturing processes [15]. In this study, an n-type <100> silicon wafer (resistivity ~ 1–10 Ωcm) with 50 nm thick thermally grown SiO2 layer on top was used as the substrate for device fabrication. Before the deposition, the substrates were cleaned in an ultrasonic bath followed by thorough washing with acetone, isopropyl alcohol and de-ionized water for 10 min each. Finally the substrate was dried and loaded in the thermal evaporator (Fillunger TCS0204 model). CuPc films were thermally evaporated at a rate of 0.1 nm/s without substrate heating, at a pressure of 10−6 Torr. Successively, 100 nm silver was thermally evaporated through a shadow mask, to form the source and drain. Out of several thicknesses of channel layer fabricated, the optimal thickness of the CuPc layer was 50 nm. The OFETs were fabricated with different channel widths (4 mm and 1000 μm) and different channel lengths (175 μm and 135 μm). In order to examine the improvements in the electrical properties of the OFET, the fabricated devices were annealed at different temperatures in air. The schematic representation of the fabricated device is shown in Fig. 2.

The surface morphology of the film was investigated by Field Emission Scanning Electron Microscopy (FESEM, Bruker Nova NanoSEM-450). The work function of CuPc thin films was studied by Scanning Tunneling Microscope (STM, Quazar Tech.). The electrical characterization of the OFETs was done in air at room temperature and different annealing temperatures using a 4-point probe station connected to an Agilent B2900A semiconductor parameter analyzer.

3. Results and discussion

3.1. Morphology of the CuPc films

Fig. 3 (a) shows the secondary electron images of CuPc thin films deposited on silicon substrates at room temperature. The surface of the film appears to consist of nano-sized spherical particles with an average size of 30 nm. STM was employed to image the CuPc layer deposited on ITO surface and to estimate its work function. The STM images of the CuPc shown in Fig. 3 (b,c) were measured at a tip-sample bias of −1.5 V and 120 pA tunneling current. The dark regions distributed throughout the image are CuPc molecules stacked on top of each other [16,17]. The tunneling current (I) to tip/sample distance (z) spectrum was taken to determine the work function CuPc, shown in Fig. 3 (d). The current is related to the tip/sample distance by the following relation [18]:

\[ I = I_0 \exp(-2zd) \]  

(1)

Where \( d \) is the tunneling distance and \( k \) is the decay constant given by \( k = \sqrt{2m}\phi/h^2 \). Here, \( \phi \) is the measured total potential. For a tip of work function \( \phi_t \) and tunneling current measured at a voltage \( V \), the work function \( \phi_s \) of the sample will be [19]

\[ \phi = (\phi_s - eV + \phi_t)/2 \]  

(2)

The value of work function measured is 4.89 ± 0.58 eV.

3.2. Electrical characterization

Since the estimated work function of CuPc is 4.89 eV, silver was used as the source and drain contacts to minimize the threshold shift. The conductivity of CuPc increases with increasing

Fig. 2. Schematic representation of OFET with CuPc as the channel layer.
temperature and this is a typical behavior of semiconductors [8].

First, we focus on the effects of annealing temperatures on the fabricated OFET devices. Fig. 4 shows the transfer characteristics of the CuPc based OFET with and without annealing with a channel length of 135 μm and a channel width of 4 mm (L/W = 0.034). The device shows reasonably good transfer behavior with evident saturation and gate dependent drain-source current. The transfer characteristics show that CuPc behaves as a p-type semiconductor.

Fig. 5 is the output characteristics of the same device, showing clear gate dependence. The non-saturating behavior is due to the space-charge limited current (SCLC) dominating over the saturation current. The sample annealed at 80 °C shows better saturation, which could be due to less defects in the film after annealing. Though the work functions of silver and CuPc are matching, a shift of approximately 2 V in the threshold voltage is seen in the output characteristics of the devices, which could be due to Ag/CuPc interfacial imperfections and series resistance due to thin Ag electrodes. The work function of silver is 4.2 eV. So according to Mott–Schottky vacuum level alignment scheme [20,21] there would be a barrier exist for holes at CuPc/Ag interfaces.

The field effect mobility was calculated from the transconductance plot shown in Fig. 4. The field effect mobility is then extracted using the standard equation:

$$\mu = \frac{L}{W C_{ox} V_{ds} g_m}$$

(3)

where $g_m$ is the transconductance, the derivative of the linear part of transfer characteristics and $C_{ox}$ is the oxide capacitance per unit area. The gate oxide capacitance ($C_{ox}$) of SiO₂ film was calculated using the formula $C_{ox} = \varepsilon A/d$, where $\varepsilon$ is the dielectric constant, $A$ is the area of the capacitor and $d$ is the thickness of the oxide layer. Then the $C_{ox}$ per unit area was directly measured using Si/SiO₂/Al capacitors, yielding an average value of 43 pF/mm². The on-off ratio of the drain current for the sample without annealing was $10^2$, which increased to $10^3$ for samples with CuPc annealed at 50 °C and $10^5$ for annealing at 80 °C. For CuPc based OFETs, Chaur et al. have reported field effect mobilities ranging from $10^{-3}$ to 1.0 cm²/V, the value depending upon the gate dielectric material, deposition technique and operating conditions [22]. In our case, the highest

![Fig. 3](image1.png)

Fig. 3. (a) Secondary electron micrograph of CuPc, (b) STM images of copper phthalocyanines on ITO surface with tunneling conditions of −1.5 V and 120 pA, (c) STM images of copper phthalocyanines on ITO surface with tunneling conditions of −1.5 V and 120 pA, (d) The I-z spectra measured on CuPc surface, from which the work function was estimated.

![Fig. 4](image2.png)

Fig. 4. Transfer curves of CuPc based OFETs with L/W of 0.034, fabricated using CuPc layer (a) as deposited, (b) annealed at 50 °C and (c) annealed at 80 °C.
mobility of 1.30 ± 0.02 cm²/V was obtained from the OFET with channel length and width of 175 µm and 1000 µm respectively, for the device layer annealed at 80 °C. The field effect mobility increased with increasing annealing temperature and increasing L/W ratios. This value is relatively higher than that obtained in the CuPc based OFETs prepared in the previous works. Yakuphanoglu et al. [23] reported a CuPc based OFET was fabricated using SiO₂ as gate dielectric. They obtained a field effect mobility of 5.32 × 10⁻³ cm²/V. Hussein et al. [8] reported that top contact CuPc based OFET with Al as the source/drain electrode onto the heavily n-doped Si substrate with an oxide layer of 60 nm. The calculated mobility value in their devices was 1.22 × 10⁻³ cm²/V. Similarly a mobility of 1.5 × 10⁻² cm²/V was obtained for 40 nm thick thermally evaporated CuPc active layers on the surface treated SiO₂ gates in the top-contact OFETs [24]. Huanqin et al. [25] have reported a large hole mobility of 0.05 cm²/V for the OFET in combination with a buffer layer and electrode modified layer together with CuPc. However, the hole mobility we report in this work shows a significant improvement over all these reported mobilities. This improvement may be a consequence of the smaller dielectric thickness or the larger L/W ratio of the present device. One of the previous works has demonstrated that the drain current increases with decreasing the thickness of the dielectric material [26]. This behavior is also similar to one observed for the multilayer dielectric based OFETs [11]. Besides, we observed that the CuPc based OFET device shows significant low drive voltage in our case compared with the values presented by other workers [26].

The extrapolation of fitted straight line of √ldi versus V_{gs} plot gives the threshold voltage. From Fig. 6 the minimum value of the threshold voltage measured is −2 V for CuPc treated at 80 °C with channel length and width of 135 µm and 4 mm respectively.

The subthreshold swing (SS) of the device is given by [13]

\[
SS = \left( \frac{d \log I_{ds}}{dV_{gs}} \right)^{-1} \quad (4)
\]

The estimated subthreshold swing of the same device is 0.69 ± 0.05 V/decade for 80 °C annealing, when measured at V_{ds} of −5 V. From the subthreshold swing, the interface trap density was estimated using the equation [27]:

\[
SS = \frac{kT}{q} \ln(10) \times \frac{qN_{it}}{C_{ox}} \quad (5)
\]

where N_{it} is the interface trap density of the device. The calculated N_{it} values are 5.14 ± 0.39 × 10¹¹ cm⁻²eV⁻¹ for the case of without annealing, 3.26 ± 0.04 × 10¹¹ cm⁻²eV⁻¹ for 50 °C treated sample and 2.41 ± 0.05 × 10¹¹ cm⁻²eV⁻¹ for 80 °C treated sample. From the results, it is clear that OFETs operated in the high temperature regime shows better performance. In addition, the transistors kept in ambient conditions were stable, when measured after duration of one week.

The L/W ratio of CuPc based OFET also affected the subthreshold swing and interface trap density. Fig. 7 shows the mobilities of the OFETs under different L/W ratios with a constant drain source voltage of −5 V. The device shows a linear reduction in mobility upon decreasing the L/W ratio. From Fig. 8, comparison of SS and N_{it} of CuPc based OFET with different L/W ratios are examined. The subthreshold slope of the device became steeper with the L/W ratio while the interface trap density slightly decreased. These results suggest that increasing the L/W ratio is an effective way to keep a minimum value of subthreshold swing.

![Fig. 5. Output characteristics of CuPc based OFETs with L/W of 0.034, fabricated using CuPc layer (a) as deposited, (b) annealed at 50 °C, and (c) annealed at 80 °C.](image)

![Fig. 6. Threshold voltage calculation of CuPc based OFETs with a channel length of 135 µm and a channel width of 4 mm.](image)

![Fig. 7. Dependence of the measured field effect mobilities of the CuPc based OFETs with and without annealing with different L/W ratios.](image)
4. Conclusion

The electrical performances of vacuum deposited thin film based p-channel OFETs with CuPc as the channel layer were studied using OFETs with bottom-gate, top-contact configuration. STM studies on the CuPc layer show an evenly deposited on/off current ratio of 3.08. These OFETs exhibit excellent transfer parameters with field effect mobility of $1.30 \pm 0.02 \text{cm}^2/\text{V}s$, on/off current ratio of $3.08 \times 10^5$, subthreshold swing of 0.51 ± 0.15 V/decade and threshold voltage close to 2 V. These operating parameters show that CuPc based OFETs can be promising for scalable, low-power flexible electronics applications.

References


